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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/970,013	10/02/2001	Noriaki Sakamoto	10417-102001	9407

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EXAMINER	
KEBEDE, BROOK	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 10/15/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/970,013	SAKAMOTO ET AL.	
	Examiner	Art Unit	
	Brook Kebede	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *14 July 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Allowable Subject Matter

1. The indicated allowability of claims 1-23 is withdrawn in view of the newly discovered reference(s) to Sakamoto et al. (US/6,531,370) and Sakamoto et al. (US/6,548,328). Rejections based on the newly cited reference(s) follow.

Priority

2. Should applicant desire to obtain the benefit of foreign priority under 35 U.S.C. 119(a)-(d) prior to declaration of an interference, a translation of the foreign application should be submitted under 37 CFR 1.55 in reply to this action.

Specification

3. The disclosure is objected to because of the following informalities:

It is noted that there are number of co-pending applications filled related to the instant application. However, the applicants fail to disclose the co-pending applications that related to the instant application as required under 37 CFR 1.56. "Information relating to or from co-pending United States Patent applications, the individuals covered by 37 CFR 1.56 have a duty to bring to the attention of the examiner, or other Office official involved with the examination of a particular application, information within their knowledge as to other co-pending United States applications which are "material to patentability" of the application in question. As set forth by the court in Armour & Co. v. Swift & Co., 466 F.2d 767, 779, 175 USPQ 70, 79 (7th Cir. 1972)." Therefore, applicants are requested to provide the serial numbers of all the co-pending application that related to the instant application.

Double Patenting

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 1-27 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-32 of U.S. Patent No. 6,531,370. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following reasons:

Re claims 1-27, the instant application claimed limitations essentially claimed in the U.S. Patent 6,531,370. The claimed subject matter contains in U.S. Patent 6,531,370 includes "preparing a conductive foil and forming an isolation trench having a smaller thickness than that of the conductive foil on the conductive foil in a region excluding where a conductive pattern of a first layer is to be formed, thereby forming the conductive pattern of the first layer; forming an interlayer insulating film over the conductive pattern of the first layer; forming plural layers of a conductive pattern on the conductive pattern of the first layer through the interlayer insulating film; mounting a circuit element onto the conductive pattern covering the circuit element and entirely molding with an insulating resin; and removing the conductive foil in a portion where the isolation trench is not provided," as recited in claim 1, "preparing a conductive foil;

providing an interlayer insulating film over the conductive foil; providing plural layers of a conductive pattern over the interlayer insulating film; mounting a circuit element onto the conductive pattern; covering the circuit element and molding a whole surface with an insulating resin; and removing the conductive foil," as recited in claim 13.

In addition, the claimed subject matter of claims 2-12 and 14-27 are also within the scope of claims 1-32 of U.S. Patent 6,531,370.

Claims 2-12 and 14-27 are also rejected as being dependent of the rejected independent base claim.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-27 are rejected under 35 U.S.C. 102(e) as being anticipated by Sakamoto et al. (US/6,548,328).

Re claim 1, Sakamoto et al. disclose a method of manufacturing a circuit device comprising the steps of: preparing a conductive foil (60) and forming an isolation trench (54) having a smaller thickness than that of the conductive foil (60) on the conductive foil (60) in a region excluding where a conductive pattern of a first layer is to be formed, thereby forming the conductive pattern of the first layer (see Figs. 3-5A); forming an interlayer insulating film (50) over the conductive pattern of the first layer; forming plural layers of a conductive pattern on the

conductive pattern of the first layer through the interlayer insulating film; mounting a circuit element onto the conductive pattern covering the circuit element and entirely molding with an insulating resin; and removing the conductive foil in a portion where the isolation trench is not provided (see Figs. 3-29).

Re claim 2, as applied to claim 1 above, Sakamoto et al. disclose all the claimed limitations including the step of separating the insulating resin through dicing for each circuit device including the circuit element (see Figs. 3-29).

Re claim 3, as applied to claim 1 above, Sakamoto et al. disclose all the claimed limitations including the limitation wherein the conductive foil is constituted by any of copper, aluminum and iron-nickel (see Figs. 3-29).

Re claim 4, as applied to claim 1 above, Sakamoto et al. disclose all the claimed limitations including the limitation wherein the isolation trench to be selectively formed on the conductive foil is provided through chemical or physical etching (see Figs. 3-29).

Re claim 5, as applied to claim 1 above, Sakamoto et al. disclose all the claimed limitations including the limitation wherein a thermosetting resin is used for the interlayer insulating film (see Figs. 3-29).

Re claim 6, as applied to claim 5 above, Sakamoto et al. disclose all the claimed limitations including the limitation wherein a via hole is formed on the interlayer insulating film through a laser (see Figs. 3-29).

Re claim 7, as applied to claim 1 above, Sakamoto et al. disclose all the claimed limitations including the limitation wherein a photosensitive resist layer is used for the interlayer insulating film (see Figs. 3-29).

Re claim 8, as applied to claim 7 above, Sakamoto et al. disclose all the claimed limitations including the limitation wherein a via hole is formed on the interlayer insulating film through photo sensitization (see Figs. 3-29).

Re claim 9, as applied to claim 1 above, Sakamoto et al. disclose all the claimed limitations including the limitation wherein the conductive pattern of the layers is formed by a copper plated layer (see Figs. 3-29).

Re claim 10, as applied to claim 9 above, Sakamoto et al. disclose all the claimed limitations including the limitation wherein the copper plated layer is formed by electroless plating and electroplating (see Figs. 3-29).

Re claim 11, as applied to claim 1 above, Sakamoto et al. disclose all the claimed limitations including the limitation wherein the circuit element has either or both of a semiconductor bare chip and a chip circuit component fixed thereto (see Figs. 3-29).

Re claim 12, as applied to claim 1 above, Sakamoto et al. disclose all the claimed limitations including the limitation wherein the insulating resin is molded by transfer molding or potting (see Figs. 3-29).

Re claim 13, Sakamoto et al. disclose a method of manufacturing a circuit device comprising the steps of: preparing a conductive foil; providing an interlayer insulating film over the conductive foil; providing plural layers of a conductive pattern over the interlayer insulating film; mounting a circuit element onto the conductive pattern; covering the circuit element and molding a whole surface with an insulating resin; and removing the conductive foil (see Figs. 3-29).

Re claim 14, as applied to claim 13 above, Sakamoto et al. disclose all the claimed limitations including the limitation the step of isolating the insulating resin through dicing for each circuit device including the circuit element (see Figs. 3-29).

Re claim 15, as applied to claim 13 above, Sakamoto et al. disclose all the claimed limitations including the limitation wherein the conductive foil is constituted by any of copper, aluminum and iron-nickel (see Figs. 3-29).

Re claim 16, as applied to claim 13 above, Sakamoto et al. disclose all the claimed limitations including the limitation wherein a thermosetting resin is used for the interlayer insulating film (see Figs. 3-29).

Re claim 17, as applied to claim 16 above, Sakamoto et al. disclose all the claimed limitations including the limitation wherein a via hole is formed on the interlayer insulating film through a laser (see Figs. 3-29).

Re claim 18, as applied to claim 13 above, Sakamoto et al. disclose all the claimed limitations including the limitation wherein a photosensitive resist layer is used for the interlayer insulating film (see Figs. 3-29).

Re claim 19, as applied to claim 18 above, Sakamoto et al. disclose all the claimed limitations including the limitation wherein a via hole is formed on the interlayer insulating film through photo sensitization (see Figs. 3-29).

Re claim 20, as applied to claim 13 above, Sakamoto et al. disclose all the claimed limitations including the limitation wherein the conductive pattern of the layers is formed by a copper plated layer (see Figs. 3-29).

Re claim 21, as applied to claim 20 above, Sakamoto et al. disclose all the claimed limitations including the limitation wherein the copper plated layer is formed by electroless plating and electroplating (see Figs. 3-29).

Re claim 22, as applied to claim 13 above, Sakamoto et al. disclose all the claimed limitations including the limitation wherein the circuit element has either or both of a semiconductor bare chip and a chip circuit component fixed thereto (see Figs. 3-29).

Re claim 23, as applied to claim 13 above, Sakamoto et al. disclose all the claimed limitations including the limitation wherein the insulating resin is molded by transfer molding or potting (see Figs. 3-29).

Re claim 24, as applied to claim 1 above, Sakamoto et al. disclose all the claimed limitations including the limitation wherein a thickness of said conductive foil is 70 to 300 μm (see Figs. 3-29).

Re claim 25, as applied to claim 13 above, Sakamoto et al. disclose all the claimed limitations including the limitation wherein a thickness of said conductive foil is 70 to 300 μm (see Figs. 3-29).

Re claim 26, as applied to claim 1 above, Sakamoto et al. disclose all the claimed limitations including the limitation wherein the circuit element is a face down semiconductor element (see Figs. 3-29).

Re claim 27, as applied to claim 13 above, Sakamoto et al. disclose all the claimed limitations including the limitation wherein the circuit element is a face down semiconductor element (see Figs. 3-29).

Response to Arguments

8. Applicants' arguments with respect to claims 1-27 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure Sakamoto et al. (US/6,545,364), Amano et al. (US/6,100,112) and Suda et al. (JP.59200427) also disclose similar inventive subject matter.

10. **THIS ACTION IS MADE NON-FINAL.**

Correspondence

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (703) 306-4511. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703) 306-2794. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Brook Kebede
October 6, 2003

W. DAVID COLEMAN
PRIMARY EXAMINER